CLAIMS

We claim:

1	A complementary metal oxide semiconductor (CMOS) device with an
2	integrated photosensitive junction field-effect transistor (JFET), the device comprising:
3	a silicon substrate;
4	\a JFET formed on a surface of the silicon substrate, the JFET including a
5	photo-absorbing layer formed on the surface of the silicon substrate; and
6	an overglass layer formed over the JFET adapted to admit photons to the
<u> 7</u>	photo-absorbing layer of the JFET,
7 8 H. F. S	wherein the JFET detects incident photons admitted through the overglass
19 □	layer and produces an amplified electrical signal corresponding to the photons
10	detected.
]] 1]	2. A CMOS device as in claim 1,
2	wherein the JFET provides a relatively low corner frequency.
1	3. A CMOS device as in claim 1,
2	wherein an input refereed noise of the JFET is relatively low.
1	4. A CMOS active pixel sensor (APS) pixel supported on a substrate comprising:
2	a junction field-effect transistor (JFET) adapted to detect photons and produce
3	an amplified electrical signal corresponding to the photons detected; and

a readout switch transistor coupled to a drain terminal of the JFET.

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1		5.	A CMOS APS pixel as in claim 4,
2			wherein a source terminal of the readout switch transistor is connected to a bus
3		and a	resistor, forming a source follower circuit.
1		6.	A CMOS APS pixel as in claim 4, further comprising:
2			a first resistor connected between a gate terminal of the JFET and a drain
3		termin	nal of the readout switch transistor; and
5	AND		a second resistor connected between a source terminal of the JFET and the
<u> 5</u>	G	drain	terminal of the readout switch transistor, wherein the first and second resistors
F ∏ 6		provid	le positive feedback and laser trimmability, and
			wherein a source terminal of the readout switch transistor is connected to a bus
7 		and a	current source, forming a source follower.
1		7.	A CMOS APS pixel as in claim 4,
2			wherein the JFET is contained in a differential amplifier circuit.
1		8.	A digital camera, comprising:
2			a CMOS active pixel sensor (APS) imager providing image data, the imager
3		comp	rising:
4			an array of CMOS APS pixels comprising a plurality of junction field-
5			effect transistors (JFETs) adapted for photodetection and electrical signal
6			amplification.

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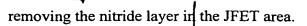
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4		forming an active region on the silicon wafer layer;
5		forming an N-well region of predetermined depth in the silicon wafer layer;
6		forming a P-well region of predetermined depth in the silicon wafer layer;
7		depositing a field oxide layer on the n-well region;
8	ار اه	implanting a dopant to form an N-channel of a desired threshold voltage in the
9	(A)	active region;
10	(A)	implanting a dopant to form a P-channel of a desired threshold voltage in the
<u></u> 11		active region;
Д Л2 Л		depositing an oxide layer and a polysilicon layer on the wafer;
V 리3 네		etching the polysilicon layer to form a CMOS gate in the active region;
14		forming a JFET area in the active region;
는 부15 진		implanting a N lightly doped drain in the substrate;
11 12 13 14 15 16 17		implanting a P lightly doped drain in the substrate;
		forming a lightly doped drain spacer in the substrate;
18		forming an n+ contact to the n-well;
19		forming an p+ contact to the p-well;
20		activating CMOS source and drain contacts for the CMOS gates;
21		salicidizing the wafer;
22		forming a tungsten plug in the CMOS integrated circuit device; and
23		forming a metal layer on the CMOS integrated circuit device.

1	14.	A process as in claim 13, wherein the step of forming a JFET area comprises:		
2		creating and implanting a channel in the JFET area;		
3		depositing polysilicon and nitride layers for JFET gate formation on the JFET		
4	area; a	and		
5		forming a JFET gate in the JFET area.		
	ALX.			
1	15.	A process as in claim 14, the step of depositing layers for JFET gate formation		
_ 2	comprising th	ne steps of:		
近 近3		depositing a polysilicon layer on the JFET area;		
¥ 4		implanting the polysilicon layer with boron difluoride ions; and		
い 手 5 =		depositing a nitride layer on the polysilicon layer.		
	16. of:	A process as in claim 14, the step of forming a JFET gate comprising the steps		
3		etching the nitride layer; and		
4		etching the polysilicon layer.		
1	17.	A process as in claim 14, the step of creating and implanting a channel in the		
2	JFET area comprising the step of:			
3		depositing an oxide layer in the JFET area.		
4 5	18.	The process as in claim 14, the step of activating CMOS source and drain		
6	contacts comp	prising the step of:		
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19. A process as in claim 13, further comprising the step of:

forming a CMOS APS imager from the CMOS integrated circuit device.